EAST - [10798960.wsp:1]

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  - L1: (2) (MOSFET or NMOS or PMOS) and (improv$3 with (charge near mobility charge near carrier nea...
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  - L3: (54) (MOSFET or NMOS or PMOS) and ((charge near mobility charge near carrier near mobility))...
  - L4: (1) "3602841".PN.
  - L5: (1) "4665415".PN.
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DBs | US-PGPUB; USPAT; USC | Plurals

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(MOSFET or NMOS or PMOS) and ((charge near mobility charge near carrier near mobility)) and strain$2 and stress and gate

BRS form | IS&R form | Image | Text | HTML

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
40	☐	☐	US 6891188 B2	20050510	17	Semiconductor device including band-engineered superlattice	257/15	257/17; 257/E21.633; 257/E29.056;
41	☐	☐	US 6890808 B2	20050510	12	Method and structure for improved MOSFETs using poly/silicide gate height control	438/199	257/E21.633; 257/E21.634; 257/E21.636;
42	☐	☐	US 6882051 B2	20050419	45	Nanowires, nanostructures and devices fabricated therefrom	257/746	257/734; 257/741; 257/E23.025;
43	☐	☐	US 6878576 B1	20050412	17	Method for making semiconductor device including band-engineered superlattice	438/162	257/E21.633; 257/E29.056; 257/E29.078;
44	☐	☐	US 6869866 B1	20050322	12	Silicide proximity structures for CMOS device performance improvements	438/581	438/595
45	☐	☐	US 6855982 B1	20050215	13	Self aligned double gate transistor having a strained channel region and process therefor	257/330	257/59; 438/259; 438/270;
46	☐	☐	US 6833294 B1	20041221	19	Method for making semiconductor device including band-engineered superlattice	438/162	257/E21.633; 257/E29.056; 257/E29.078;
47	☐	☐	US 6830964 B1	20041214	18	Method for making semiconductor device including band-engineered superlattice	438/162	257/E21.633; 257/E29.056; 257/E29.078;
48	☐	☐	US 6784101 B1	20040831	9	Formation of high-k gate dielectric layers for MOS devices fabricated on strained lattice semiconductor substrates with minimized stress reli	438/666	438/197; 438/198; 438/199
49	☐	☐	US 6689671 B1	20040210	9	Low temperature solid-phase epitaxy fabrication process for MOS devices built on strained semiconductor substrate	438/486	257/E21.129; 257/E21.133; 257/E21.335;
50	☐	☐	US 6475869 B1	20021105	7	Method of forming a double gate transistor having an epitaxial silicon/germanium channel region	438/303	257/E21.415; 257/E21.442;

DAN 1.6.1 -... | EAST - [107... | EAST Brows... | EAST Brows...